

What is claimed is:

- 1 1. A circuit operable to measure leakage current in a Dynamic Random
2 Access Memory (DRAM) comprising:
3 a plurality of DRAM bit cell access transistors coupled to a common bit
4 line, a common word line, and a common storage node, wherein said access
5 transistors may be biased to simulate a corresponding plurality of inactive bit cells
6 of a DRAM; and
7 a current mirror in communication with said common storage node
8 operable to mirror a total leakage current from said plurality of bit cell access
9 transistors when said access transistors are biased to simulate said inactive bit
10 cells.
- 1 2. The circuit as recited in claim 1, wherein said access transistors are
2 selected from the group consisting of NMOS and PMOS transistors.
- 1 3. The circuit as recited in claim 1, wherein said current mirror comprises:
2 at least two transistors with respective gate nodes electrically connected to
3 said common storage node.
- 1 4. The circuit as recited in claim 3, wherein said current mirror transistors are
2 selected from the group consisting of NMOS and PMOS transistors.
- 1 5. The circuit as recited in claim 3, wherein said current mirror transistors are
2 selected to measure a multiple of said total leakage current, said multiple being
3 greater than one.
- 1 6. The circuit as recited in claim 3, wherein said current mirror comprises at
2 least two NMOS transistors coupled between said common storage node and a
3 ground node, whereby a voltage at said common storage node simulates a voltage
4 reflective of a '0' state DRAM bit cell when said access transistors are biased to

5 simulate said inactive bit cells. 7. The circuit as recited in claim 3, wherein
6 said current mirror comprises at least two PMOS transistors coupled between said
7 common storage node and a supply voltage node, whereby a voltage at said
8 common storage node simulates a voltage reflective of a '1' state DRAM bit cell
9 when said access transistors are biased to simulate said inactive bit cells.

1 8. The circuit as recited in claim 1, further comprising a plurality of storage
2 capacitors coupled to said storage node, each of said storage capacitors associated
3 with a respective one of said access transistors, wherein said current mirror is
4 operable to mirror a total leakage current from said plurality of bit cell access
5 transistors and said capacitors.

1 9. A DRAM current meter comprising:
2 a first current monitor operable to measure a leakage current associated
3 with a cell in a first state;
4 a second current monitor operable to measure a leakage current associated
5 with a cell in a second state; and
6 a current mirror in communication with said first and second current
7 monitors wherein said current mirror is operable to mirror a total leakage current
8 measured by said first and second current monitors.

1 10. The meter as recited in claim 9, wherein said second current monitor
2 provides a current to said current mirror.

1 11. The meter as recited in claim 10, wherein said current mirror is a current
2 sink for said first current monitor.

1 12. The meter as recited in claim 9, wherein each of said first and second
2 current monitors comprises:
3 a plurality of DRAM bit cell access transistors coupled to a common bit
4 line, a common word line, and a common storage node, wherein said access

5 transistors may be biased to simulate a corresponding plurality of inactive bit cells
6 of a DRAM; and
7 a current mirror in communication with said common storage node
8 operable to mirror a total leakage current from said plurality of bit cell access
9 transistors when said access transistors are biased to simulate said inactive bit
10 cells.

1 13. The meter as recited in claim 12, wherein said each current mirror of said
2 first and second current monitors comprises:
3 at least two transistors with respective gate nodes electrically connected to
4 said common storage node.

1 14. The meter as recited in claim 13, wherein said transistors of said current
2 mirrors of said first and second current monitors are selected to measure a
3 multiple of said total leakage current, said multiple being greater than one.

1 15. The meter as recited in claim 13,
2 wherein said current mirror of said first current monitor comprises at least
3 two NMOS transistors coupled between said common storage node and a ground
4 node, whereby a voltage at said common storage node simulates a voltage
5 reflective of a '0' state DRAM bit cell when said access transistors are biased to
6 simulate said inactive bit cells, and
7 wherein said current mirror of said second current monitor comprises at
8 least two PMOS transistors coupled between said common storage node and a
9 supply voltage node, whereby a voltage at said common storage node simulates a
10 voltage reflective of a '1' state DRAM bit cell when said access transistors are
11 biased to simulate said inactive bit cells.

1 16. The meter as recited in claim 12, wherein said current mirrors of said first
2 and second current monitors each further comprise:

3 a plurality of storage capacitors coupled to said storage node, each of said
4 storage capacitors associated with a respective one of said access transistors,
5 wherein said current mirror is operable to mirror a total leakage current from said
6 plurality of bit cell access transistors and said capacitors.

1 17. A Dynamic Random Access Memory (DRAM) comprising a circuit
2 operable to measure simulated leakage current in said DRAM comprising:

3 a plurality of DRAM bit cells comprising:

4 a plurality of DRAM bit cell access transistors coupled to a
5 common bit line, a common word line, and a common storage node, wherein said
6 access transistors may be biased to simulate a corresponding plurality of inactive
7 bit cells of a DRAM; and

8 a plurality of storage capacitors coupled to said storage node, each
9 of said storage capacitors associated with a respective one of said access
10 transistors; and

11 a current mirror in communication with said common storage node
12 operable to provide a multiple of a total leakage current from said plurality of bit
13 cell access transistors and said capacitors when said access transistors are biased
14 to simulate said inactive bit cells.

1 18. The DRAM of claim 17, wherein said current mirror comprises:

2 at least two transistors with respective gate nodes electrically connected to
3 said common storage node.

1 19. The DRAM of claim 18, wherein said current mirror comprises at least
2 two NMOS transistors coupled between said common storage node and a ground
3 node, whereby a voltage at said common storage node simulates a voltage

4 reflective of a '0' state DRAM bit cell when said access transistors are biased to
5 simulate said inactive bit cells. 20. The DRAM of claim 18, wherein said
6 current mirror comprises at least two PMOS transistors coupled between said
7 common storage node and a supply voltage node, whereby a voltage at said
8 common storage node simulates a voltage reflective of a '1' state DRAM bit cell
9 when said access transistors are biased to simulate said inactive bit cells.

1 21. The DRAM of claim 17, wherein said DRAM comprises a DRAM array
2 and said circuit is fabricated proximate to said DRAM array, whereby said circuit
3 is exposed to environmental conditions substantially similar to said DRAM
4 memory array. 22. The DRAM of claim 17, wherein said multiple is greater
5 than one.